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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,537	03/12/2004	Li-Kong Wang	728-228 CON	7838

66668 7590 02/11/2008
THE FARRELL LAW FIRM - IBM
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EXAMINER

TRA, ANH QUAN

ART UNIT	PAPER NUMBER
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2816

MAIL DATE	DELIVERY MODE
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02/11/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/799,537	Applicant(s) WANG ET AL.	
	Examiner QUAN TRA	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/12/07.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 and 22-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 22-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This action is in response to the Remarks filed 12/12/07. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 25 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Pasternak (USP 6577535, previously cited) in view of Ong (USP 6732304).

Pasternak's figure 3A shows a DC voltage generator system for supplying at least one voltage level to a plurality of subsystems (304, 306 ...310), each of the subsystems having a plurality of units (it is inherent that each of the 304, 306...310 has pluralities of internal circuits), at least two of the units located in at least one of the subsystems being different from each other, the DC voltage generator system comprising: a plurality of local DC voltage generators (CP 312-318) associated with at least one unit of the plurality of subsystems, each local DC voltage generator independently supplying voltage to the at least one unit of the plurality of subsystems; and a power control unit (330) for determining a performance mode of the system and disabling the local DC voltage generators according to the performance mode, wherein a separate enabling clock signal (PE0-PE3) is supplied to each DC voltage generator and the at least one unit of the plurality of subsystems associated each DC voltage generator. Figure 3A fails to show that shown circuits are on a single chip. However, Ong's figure 2 shows a modified of figure 1. Ong's figure 2 combine plurality of chips in figure 1 on a single chip in order to save

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space. Therefore, it would have been obvious to one having ordinary skill in the art to combine Pasternak's chips on a single chip for the purpose of saving space.

3. Claims 1-12 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pasternak (USP 6577535) in view of Ong (USP 6732304) and Drouot (USP 5796285).

Pasternak's figure 3a shows all elements of the claims except for the detail of each charge pump circuit. However, Drouot's figure 1 shows a low cost charge pump circuit. Therefore, it would have been obvious to one having ordinary skilled in the art to use Drouot's charge pump circuit for each of Pasternak's charge pumps for the purpose of saving cost. Thus, the modified Pasternak's figure 3A further shows each DC voltage generator comprising: regulator system (Drouot's 5); power control unit and clock control unit (circuits in Pasternak's 302 that generates CS0 and CS1); AND gate (Pasternak's 352, 354, 356, 358); first to third transistors (Drouot's 16, 12, 11) connected as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/QUAN TRA/
Primary Examiner, Art Unit 2816